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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,048	06/24/2003	Jason J. Payne	1826-US	1882

7590 07/14/2005

Teradyne, Inc.
Legal Department
321 Harrison Avenue
Boston, MA 02118

EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/603,048	PAYNE ET AL.
	Examiner	Art Unit
	Hoa C. Nguyen	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 14-19* is/are rejected.

7)☒ Claim(s) *5 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~*24 June 2003*~~ Nov 22, 2004
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: ~~*Attach specification page 3.*~~ None

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character not mentioned in the description: 111. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

(a) The specification does not describe the reference number 113 as shown in figures 2 and 7.

(b) On page 12, line 10, there is reference number 216(b), which is not shown in figures 9 or 10 as specified in the specification.

(c) On page 12, lines 9-11, the specification initially identifies reference number 216 as "the base" and then later identifies as "the openings".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 9-12, 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuroda (U.S. Patent 5,331,514).

Regarding claim 1, Kuroda discloses a PCB having a surface providing a mating interface to which is electrically connected an electrical component having signal conductors 3S(3) and ground conductors 3G(3), see figure 2 and column 2, lines 28-32. The PCB comprising:

(a) A plurality of stacked dielectric layers 2 with a conductor 3S(3) and 3G(3) exposed on at least one of the plurality of the layers, see figure 2, column 1, lines 41-43, and column 2, lines 44-49,

(b) a mating interface including:

(c) a plurality of conductive vias 3 aligned in a repeating pattern of a square so forming a plurality of rows of squares, see figure 5 and column 1, lines 49-52,

(d) the plurality of conductive vias 3 extending through at least a portion of the plurality of the layers 2, at least one of the plurality of conductive vias 3 intersecting the conductor, see figure 2 and column 2, line 68-continuing column 3, lines 1-8,

(e) the plurality of conductive vias 3 including signal conductor connecting conductive vias 3S and ground conductor connecting conductive vias 3G, see figure 2 and column 2, lines 44-49, and

(f) for each of plurality of rows of the conductive vias 3, there are at least twice as many ground conductor connecting conductive vias 3G as signal conductor connecting conductive vias 3S and the conductive vias 3 are positioned relative to one another so that for each signal conductor connecting conductive via 3S, there are ground conductor connecting conductive vias 3G adjacent either side of the signal conductor connecting conductive via 3S, see figures 1 and 5, and column 1, lines 49-52.

Regarding claim 9, as explained in claim 1 above and in figure 5, Kuroda discloses every limitation in claim 9 and for each of the plurality of rows of the conductive vias 3 arranged in a square pattern, each signal conductor connecting conductive via 3S has corresponding ground conductor connecting conductive vias 3G adjacent either side of the signal conductor connecting conductive via 3S so as to form a repeating pattern along the row of ground conductor connecting conductive via 3G - signal conductor connecting conductive via 3S - ground conductor connecting conductive via 3G.

Regarding claim 17, as explained in claims 1 and 9 above and in figure 5, Kuroda discloses every limitation in claim 17 including the positions of the signal conductor connecting conductive vias 3S in the first rows relative to the positions of the signal conductor connecting conductive vias 3S in the second rows are offset so that

each signal conductor connecting conductive via 3S in the first and second rows has a ground conductor connecting conductive via 3G adjacent at least three sides.

Regarding claims 2 and **10,** the vias of Kuroda can be arranged in a rectangular pattern instead of a square pattern so forming rows of vias along the width sides of the rectangular, see figure 5 and column 4, lines 9-17. Since the width of a rectangular is shorter than the length, therefore the distance between the signal conductor connecting conductive via 3S and the adjacent ground conductor connecting conductive via 3G of a row is always less than the distance between adjacent rows of the conductive vias 3.

Regarding claims 3, 11 and **18**, as explained in claim 9 above, the distance between a signal conductor connecting conductive via 3S and an adjacent ground conductor connecting conductive via 3G on one side is similar to a distance between the signal conductor connecting conductive via 3S and an adjacent ground conductor connecting conductive via 3G on the other side.

Regarding claims 4, 12, and **19**, Kuroda discloses a surface mounting pad disposed on each of the plurality of conductive vias 3, the signal conductor 3S(3) and ground conductor 3G(3) of the electrical component being electrically connected to the surface mounting pads. The surface mounting pads are the top conductive surface of the vias that the component is attached to, see figure 2.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-8 and14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda in view of Uematsu et al. (U.S. Patent 6,787,710 B2).

(a) Kuroda teaches a PCB as explained above with respect to claims 1-4, 9-12, and 17-19, but failed to disclose ground and power planes.

(b) Uematsu et al. teaches a PCB having conductive vias 10 and 11 extending through a multilayer substrate, which includes a power voltage plane layer 1, a ground plane layer 2, and an area 12 surrounding the vias that is free of the layers, see figure 1 and column 3, lines 10-23.

(c) It would be obvious to one skill in this art at the time of invention to have made the power plane layer 1 and the ground plane layer 2 of Uematsu et al. in the PCB of Kuroda for providing power and ground structure for Kuroda's PCB.

Regarding claims 6 and 14, as explained in 6(b) and 6(c) above, for each signal conductor connecting conductive via 3S of the ground plane layer, it would be obvious to one skill in this art at the time of invention to have made a free area 12 surrounding the signal conductor connecting conductive via 3S that is free of the ground plane layer for preventing an advertent short circuit between the signal conductor connecting conductive via 3S and the ground plane layer.

Regarding claims 7 and 15, as can be seen in figures 1 and 5 with free areas 12 surrounding the signal conductor connecting conductive vias 3S as explained in 6(b) above, each ground conductor connecting conductive via 3G of the ground plane layer,

there is always at least one discrete area adjacent the ground conductor connecting conductive via 3G that is free of the ground plane layer.

Regarding claims 8 and 16, as explained in 6(b) and 6(c) above, for each signal conductor connecting conductive via 3S and its corresponding adjacent ground conductor connecting conductive vias 3G extending through the power voltage plane layer, it would be obvious to one skill in this art at the time of invention to have made a free area 12 surrounding the conductive vias that is free of the power plane layer for preventing an advertent short circuit between the conductive vias and the power voltage plane layer.

Allowable Subject Matter

7. Claims 5 and 13 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all the limitations of the base claims and any intervening claims.

Citation of Relevant Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Arndt et al (U.S. Patent 6,232,564 B1) discloses a printed wiring board wireability enhancement.

McNamara et al (U.S. Patent 6,537,087 B2) discloses an electrical connector.

Park et al (U.S. Patent 6,815,621 B2) discloses a chip scale package, printed circuit board, and method of designing a printed circuit board.

Yamasaki (U.S. Patent 6,609,933 B2) discloses a shield connector, which effectively suppresses cross talk.

Rothermel et al. (U.S. Patent 6,384,341) discloses a differential connector footprint for a multilayer circuit board.

Horiuchi et al. (U.S. Patent 6,194,668 B1) discloses a multi-layer circuit board.

Kametani et al. (U.S. Patent 5,590,030) discloses a circuit board capable of efficiently conducting heat through an inside thereof using thermal lands surrounding through-hole connections.

Smith (U.S. Patent 4,859,806) discloses a discretionary interconnect.

Sherman (U.S. Patent 5,784,262) discloses an arrangement of pads and through-holes for semiconductor packages.

Stokoe (U.S. Patent 6,293,827) discloses a differential signal electrical connector.

Jessep et al. (Pub. No.: U.S. 2003/0091730 A1) discloses via shielding for power/ground layers on printed circuit board.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
6 July 2005

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